ABSTRACT OF THE DISCLOSURE

**[0080]** Methods and Apparatuses for generating and distributing a clock signal between components within a semiconductor chip. According to one embodiment of the invention, a clock generator, distributed over an integrated circuit, includes a plurality of cells each coupled to multiple adjacent ones of the plurality of cells by different clock wires; wherein, for each of the plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge. According to another embodiment of the invention, an integrated circuit includes a distributed clock generator and a plurality of sets of synchronous logic. The distributed clock generator includes a plurality of cells and a plurality of clock wires. The plurality of clock wires each couple together two of said plurality of cells such that said plurality of cells are coupled together in grid. The plurality of cells, responsive to a mixing of previous clock edges produced by at least certain of said plurality of cells, detect when to produce the next clock edge. The plurality of sets of synchronous logic each have a clock input. Each clock input of each of these sets is coupled to a different one of said plurality of clock wires.